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OUT A CELL SEARCH
PROCESSING AT A HIGH SPEED

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Sir:

Transmitted herewith for filing under 37 C.F.R. § 1.53(b) is the nonprovisional utility patent application of:

Koichi TAMURA

Enclosed are:

- Specification, Claim(s), and Abstract (35 pages).
- Formal drawings (4 sheets, Figures 1-4).
- Declaration and Power of Attorney (4 pages).
- Assignment of the invention to NEC CORPORATION.
- Assignment Recordation Cover Sheet.
- Claim for Convention of Priority and priority document.
- Small Entity statement.
- Information Disclosure Statement.
- Form PTO-1449 with copies of 4 listed reference(s).

The filing fee is calculated below:

	Claims as Filed	Included in Basic Fee	Extra Claims	Rate	Fee Totals
Basic Fee				\$690.00	\$690.00
Total Claims:	18	- 20	= 0	x \$18.00	= \$0.00
Independents:	12	- 3	= 9	x \$78.00	= \$702.00
If any Multiple Dependent Claim(s) present:				+ \$260.00	= \$0.00
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[]	Assignment Recording Fee per property			\$40.00	\$40.00
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The required filing fees are not enclosed but will be submitted in response to the Notice to File Missing Parts of Application.

The Assistant Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Assistant Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741.

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CELL SEARCH METHOD IN CDMA CAPABLE OF CARRYING OUT
A CELL SEARCH PROCESSING AT A HIGH SPEED

Background of the Invention:

This invention relates to a cell search method in a code division multiple access (CDMA) system.

In the manner which is well known in the art, a code division multiple access (CDMA) system is one of multiple access system techniques in a cellular system (mobile communication system) such as a mobile telephone system and a portable telephone system used when a plurality of stations simultaneously carry out communications by using the same frequency band. On the other hand, a frequency division multiple access (FDMA) system, a time division multiple access (TDMA) system, and so on, are used as other multiple access system techniques other than the CDMA system. In comparison with the other multiple access techniques, the CDMA system is advantageous in that it is possible to achieve a high frequency utilization efficiency and is possible to accommodate more users.

The CDMA system carries out multiple access by a spread spectrum communication which transmits a spectrum of an information signal by spreading the spectrum of the information signal into a wide band sufficiently wider than an original information band width.

The cellular system (mobile communications system) generally comprises a mobile communications terminal (which is also called a "mobile station") MS and a plurality of base stations BS each of which attends to a cell. The CDMA system is adopted as an access system for third-generation mobile communication systems. In the CDMA system, the mobile station MS carries out, as a handover in a case where the mobile station MS moves between a moving source cell and a moving destination cell, a soft handover which combines an electric wave signal from a base station BS in the moving source cell with another electric wave signal from another base station BS in the moving destination cell. In order to perform the soft handover, the mobile station MS must carry out a cell search which searches the base station BS in the moving destination cell. That is, the "cell search" or a "cell search processing" means that the mobile station MS detects a connected cell.

In addition, in the CDMA system, in order to increase a capacity by suppressing and preventing transmission and reception of interference signals, sectorization (a directivity control technique) for dividing each cell into a plurality of sectors is carried out.

Although each base station always transmits a radio signal via a radio channel called a perch channel, the radio signal on the perch channel is transmitted using a peculiar spreading code in each cell (base station). Accordingly, each base station informs, using the perch channel, the mobile station of a spreading code used in peripheral cells of its own station. The mobile station periodically measures line

quality (signal-to-interference ratio (SIR)) of a radio channel (the perch channel of the peripheral cells) which uses the informed spreading code and informs a network of a measured result. Such an operation is called a peripheral cell search. As a result, the network can determine that to which cell the mobile station is moving.

In prior art, the above-mentioned cell search processing is a processing which is necessary to the mobile station MS on starting communication. That is, if the spreading code and a spreading timing are not established by the cell search, the mobile station MS cannot carry out a demodulation processing. As a result, rapidness of the cell search processing is one of techniques desired in communications in the CDMA system.

In addition, various preceding arts related to the present invention are already known. By way of example, Japanese Unexamined Patent Publication of Tokkai No. Hei 9-271,071 or JP-A 9-271071 describes "MOBILE COMMUNICATION EQUIPMENT" to shorten the initial synchronization of a mobile station, time requiring the judgement of existence in a range and long code synchronous acquisition time in a cellular system using a CDMA (code division multiple access)/TDD (time division duplex) system. The mobile communication equipment described in JP-A 9-271071 comprises a receiving base-band processing part, a synchronizing circuit, a receiving level detection circuit. The receiving base-band processing part reproduces the data of a perch channel from a received signal by using symbol timing obtained from the synchronizing circuit. The synchronizing circuit detects a unique word from the data of

the perch channel and executes slot synchronous acquisition. The receiving level detection circuit judges, as the nearest base station, a base station using a short code having the highest receiving level out of obtained receiving levels. The base station inserts information related to frame timing and information related to a long code sort used for an outgoing communication channel into the perch channel and transmits these information. The synchronizing circuit receives the transmitted information, acquires frame synchronization and acquires long code synchronization by using the long code sort.

In addition, Japanese Unexamined Patent Publication of Tokkai No. Hei 10-126,830 or JP-A 10-126830 describes "MOBILE COMMUNICATION TERMINAL" to detect the change of receiving quality of peripheral cells and to instruct the soft handover to a mobile communication terminal by adding a receiving level measurement means to the mobile communication terminal to measure the receiving level of the signal received in a receiving band before the adverse diffusion in addition to a peripheral cell search constitution. In JP-A 10-126830, a mobile communication station acquires the spread code information which is used by peripheral cells and stores it in a spread code storage means. A peripheral cell search control means sets a cell search execution cycle and a receiving level measurement execution cycle to first and second timers, respectively. When the second timer counts up its counting, the peripheral cell search control means instructs a receiving level measurement means to measure the receiving level and decides the value of RSSI change of a signal included in a

receiving band based on the measurement result of the receiving level measurement means. If the RSSI change is large, the spread codes which are used by the peripheral cells stored in the spread code storage means are successively set to a sequential inverse spread means. Then a receiving quality measurement means measures the SIR received from every peripheral cell.

Furthermore, Japanese Unexamined Patent Publication of Tokkai No. Hei 10-164,021 or JP-A 10-164012 discloses "CELL SEARCH CIRCUIT FOR CDMA" to improve an S/N and to suppress the increase of search time and a circuit scale by synchronously adding the time integral results of signals accumulated in a ring buffer and controlling the shift operation of a diffusion signal generator having a phase shift function based on the result. That is, the cell search circuit for CDMA disclosed in JP-A 10-164012 comprises a spreading signal generation circuit with a phase shift function, a multiplier for multiplying the output of the spreading signal generation circuit by an input signal, and a ring buffer for accumulating correlation results for the number of synchronous adding times for synchronous-adding the plural signals. A buffer for one signal in the ring buffer and an adder constitute an accumulator and it integrates time in the same degree as unit signal continuing time before spreading. Synchronous addition is to add time integral results for respective signals accumulated in the ring buffer by the combination of polarities which are previously decided, to judge the synchronous state of the spreading codes based on a synchronous addition result and to

a synchronous shift operation when synchronism is not established so as to acquire synchronism.

In addition, Japanese Granted Patent Publication of No. 2,861,985 or JP-B 2861985 discloses "HIGH SPEED CELL SEARCHING SYSTEM FOR CDMA" to enable cell search at a high speed by making data obtained by forming an orthogonal code through the use of a polarity of plural symbols spread by a spreading signal as a down signal and performing common-mode addition by means of a correlation device with the combination of polarities codes extending the plural symbols at the time of detecting. In JP-B 2861985, a correlating part is provided with a short code generating circuit and outputs a correlated value obtained by the correlating device to a ring buffer for common-mode addition by RAM. The buffer common-mode-adds the combination of the polarities the orthogonal code can make by an orthogonal code polarity control circuit inside a maximum value detecting circuit. The common-mode-added value of a group I and a group Q obtained as the result is transformed to power by a square sub circuit to be added to the maximum value detecting circuit and a chip counter and a symbol counter houses a chip position and a symbol position with maximum values and the polarity of the orthogonal code at the time in a maximum value register and outputs residual values to a long code identifier.

Now, attention will be directed to a case where the mobile station MS does not hardly move on starting communication from an end of previous communication and the mobile station MS lies in the same sector (or the same cell). In this event, the processed result of the cell search hardly should not change

in the mobile station MS. However, as described above, the prior art performs the cell search processing in the mobile station MS on starting communication. Such an unnecessary cell search processing merely delays an acquisition of the cell search result and it results in increasing of consumed power.

On the other hand, any of the above-mentioned publications takes no thought of conditions regarding the case where the mobile station MS restarts communication with almost no moving, in the similar manner as the prior art.

Summary of the Invention:

It is therefore an object of this invention to provide a cell search method for a CDMA, which is capable of carrying out a cell search processing at a high speed by using a previous cell search result.

It is another object of this invention to provide a cell search method for CDMA of the type described, which is capable of decreasing consumed power in the cell search processing.

Other objects of this invention will become clear as the description proceeds.

In order to achieve the above-mentioned objects, this invention adopts technical structure as follows.

That is, according to an aspect of this invention, a cell search method in a CDMA system comprises the step of carrying out a cell search processing by using cell search result information on previous communication.

According to another aspect of this invention, a cell search method in a CDMA system comprises the steps of storing,

on ending communication, a perch channel spreading code in a memory part, and of carrying out, on starting the next communication, a cell search processing by using the perch channel spreading code stored in the memory circuit.

According to still another aspect of this invention, a cell search method in a CDMA system comprises the steps of starting a timer on ending communication, of determining, by watching a timer value of the timer on starting the next communication, whether or not the timer value is not less than a communication stop time interval threshold value, and of carrying out a cell search processing using a cell search result on previous communication when the timer value is less than the communication stop time interval threshold value.

According to yet another aspect of this invention, a cell search method in a CDMA system comprises the steps of monitoring a communication stop time interval and of carrying out a cell search processing using a previous cell search result when the communication stop time interval is shorter than a threshold time interval.

According to a further aspect of this invention, a cell search method in a CDMA system comprises the steps of monitoring a communication stop time interval, of carrying out a cell search processing using a previous cell search result when the communication stop time interval is shorter than a first threshold time interval, and of carrying out a cell search processing using the previous cell search result in consideration of a timing offset between respective sectors when the communication stop time interval is not shorter than

the first threshold time interval and is shorter than a second threshold time interval.

According to a still further aspect of this invention, a cell search method in a CDMA system comprises the steps of monitoring a communication stop time interval and of carrying out a cell search processing using a previous cell search result in consideration of a timing offset between respective sectors when the communication stop time interval is shorter than a threshold time interval.

Brief Description of the Drawing:

Fig. 1 is a block diagram of a main part (a cell search circuit) of a mobile station which realizes a cell search method in a CDMA system according to a first embodiment of this invention;

Fig. 2 is a flow chart for use in describing the cell search method of the CDMA system according to the first embodiment of this invention;

Fig. 3 is a flow chart for use in describing a cell search processing; and

Fig. 4 is a block diagram of a main part (a cell search circuit) of a mobile station which realizes a cell search method in a CDMA system according to a second embodiment of this invention.

Description of the Preferred Embodiment:

Referring to Fig. 1, the description will proceed to a main part (a cell search circuit) in a mobile station MS that

realizes a cell search method according to a first embodiment of this invention. The illustrated mobile station MS or the cell search circuit comprises a delay profile calculating circuit 12, a spreading code and spreading timing detecting circuit 13, a received data processing circuit 14, a spreading code and spreading timing memory circuit 15, a known signal replica generating circuit 16, and a timer 17.

The delay profile calculating circuit 12 and the received data processing circuit 14 are connected to an orthogonal detector (not shown). The delay profile calculating circuit 12 is connected to the spreading code and spreading timing detecting circuit 13, the spreading code and spreading timing memory circuit 15, and the known signal replica generating circuit 16. The spreading code and spreading timing detecting circuit 13 is connected to the received data processing circuit 14, the spreading code and spreading timing memory circuit 15, and the known signal replica generating circuit 16. The received data processing circuit 14 is connected to the spreading code and spreading timing detecting circuit 13. The spreading code and spreading timing memory circuit 15 is connected to the spreading code and spreading timing detecting circuit 13, the delay profile calculating circuit 12, and the known signal replica generating circuit 16. The known signal replica generating circuit 16 is connected to the spreading code and spreading timing storing circuit 15, the timer 17, and the delay profile calculating circuit 12.

The orthogonal detector carries out an orthogonal detection on a received signal to produce an in-phase component

signal (I component signal) and a quadrature component signal (Q component signal) of a perch channel that are orthogonal detected and modulated. The I component signal and the Q component signal are supplied to the delay profile calculating circuit 12. The delay profile calculating circuit 12 is supplied with known signal replicas for N codes generated by the known signal replica generating circuit 16, a spreading code and spreading timing detected signal detected by the spreading code and spreading timing detecting circuit 13, and a spreading code and spreading timing stored signal stored in the spreading code and spreading timing memory circuit 15, where N represents a positive integer which is not less than two. The delay profile calculating circuit 12 generates, by using the known signal replicas for the N codes, N delay profiles based on the above-mentioned I component signal and the above-mentioned Q component signal to produce a delay profile signal indicative of the N delay profiles.

The delay profile signal is supplied to the spreading code and spreading timing detecting circuit 13. The spreading code and spreading timing detecting circuit 13 detects, by detecting a peak of power values in the delay profiles, a using spreading code and a using spreading timing to produce the spreading code and spreading timing detected signal indicative of the using spread code and the using spreading timing. The spreading code and spreading timing detected signal is supplied to the received data processing circuit 14, the spreading code and spreading timing memory circuit 15, and the known signal replica generating circuit 16.

When the using spreading code and the using spreading timing are detected by the spreading code and spreading timing detecting circuit 13 or responsive to the spreading code and spreading timing detected signal, the received data processing circuit 14 carries out a demodulation processing on the I component signal and the Q component signal to produce a demodulated output signal. Simultaneously, information indicative of the using spreading code and the using spreading timing is stored in the spreading code and spreading timing memory circuit 15. The spreading code and spreading timing memory circuit 15 produces the spreading code and spreading timing stored signal. The spreading code and spreading timing stored signal is supplied to the delay profile calculating circuit 12 and the known signal replica generating circuit 16.

The timer 17 is supplied with communication start/end information indicative of a start of communication or an end of communication. Supplied with the communication end information indicative of the end of communication, the timer 17 starts to count an elapsed time interval elapsed from the end of communication. The timer 17 produces the elapsed time interval or a timer value indicative of a communication stop time interval. The timer value is supplied to the known signal replica generating circuit 16.

On starting of a next communication, the known signal replica generating circuit 16 watches or monitors the timer value of the timer 17. If the timer value is not less (shorter) than a communication stop time interval threshold value T_{max} , the known signal replica generating circuit 16 generates the

known signal replicas for the N codes to make the delay profile calculating circuit 12 carry out a normal cell search processing.

When a time interval (the timer value) until start of the next communication is less (shorter) than the communication stop time interval threshold value T_{max} , the delay profile calculating circuit 12 generates, by using only one spreading code supplied from the spreading code and spreading timing memory circuit 15, a delay profile near to the spreading timing on a previous communication. By using the generated delay profile, the spreading code and spreading timing detecting circuit 13 carries out a processing of a spreading code detection and a spreading timing detection. If the spreading code and the spreading timing are not detected, the normal cell search processing is carried out.

Referring now to Fig. 2, description will be made as regards operation of the cell search circuit illustrated in Fig. 1.

When communication comes to an end caused by clear-down or disconnection due to shadowing (step S1), the timer 17 starts (step S2). The timer 17 stops when the elapsed time interval (the timer value) reaches the communication stop time interval threshold value T_{max} which is set (step S3).

When communication starts again (step S4), the known signal replica generating circuit 16 watches the timer value of the timer 17 (step S5). When the timer value is equal to the communication stop time interval threshold value T_{max} , the known signal replica generating circuit 16 resets the timer 17

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(step S9) and a combination of the known signal replica generating circuit 16, the delay profile calculating circuit 12, the spreading code and spreading timing detecting circuit 13, and the received data processing circuit 14 executes the normal cell search processing (step S10).

More specifically, in the step S10, the I component signal and the Q component signal, which are orthogonal detected and demodulated, are supplied to the delay profile calculating circuit 12. In order to carry out a processing illustrated in Fig. 3 which will later be described, the known signal replica generating circuit 16 successively generates a first search code replica, a second search code candidate replica, and a scramble code candidate replica. The delay profile calculating circuit 12 calculates a power delay profile by using an orthogonal detected output and a known signal replica and the spreading code and spreading timing detecting circuit 13 successively processes a slot timing establishment, a second search code group establishment, and a use scramble code establishment. When the scramble code establishment is made by the spreading code and spreading timing detecting circuit 13, the received data processing circuit 14 demodulates the I component signal and the Q component signal of the perch channel and spreading code and spreading timing information is stored in the spreading code and spreading timing memory circuit 15.

On the other hand, if the timer value of the timer 17 is less (shorter) than the communication stop time interval threshold value T_{max} at the step S5, the known signal replica generating circuit 16 stops and resets the timer 17 (step S6)

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and generates, on the basis of information stored in the spreading code and spreading timing memory circuit 15, a spreading code used on previous communication. The delay profile calculating circuit 12 calculates, by using the spreading code produced by the known signal replica generating circuit 16, the delay profile near to the previous communication spreading timing produced by the spreading code and spreading timing memory circuit 15. A processing after that is similar to the normal cell search processing and the spreading code and spreading timing detecting circuit 13 attempts the scramble code establishment (step S7).

When the scramble code establishment is made or when the perch channel is detected (YES in a step S8), the received data processing circuit 14 executes demodulation of the I component signal and the Q component signal of the perch channel and stores the spreading code and spreading timing information in the spreading code and spreading timing memory circuit 15 (step S11). If the scramble code establishment is not made in the previous used spreading code and spreading timing (NO in the step S8), the normal cell search processing is started (the step S10).

Fig. 3 illustrates a flow chart of the cell search processing. The normal cell search processing detects one timing from timing candidates which are equal in number to [256(chips) x 10(symbols) x 16(slots) x (the number of over-sampling)] at a step S21. The step S21 is followed by a step S22 at which the normal cell search processing detects one group from thirty-two groups for the second search code at a detected timing of the step S21. The step S22 proceeds to a

step S23 at which the normal cell search processing detects, from thirty-two scramble codes in the detected group at the step S22, a particular scramble code assigned to its own cell (sector).

That is, in the normal cell search processing, candidates for establishing a spread code and a spreading timing are equal in number to [256(chips) x 10(symbols) x 16(slots) x (the number of the over-sampling) x 32(second search code groups) x 32(scramble codes/groups)].

On the other hand, according to this invention, it is possible to decrease the candidates to [1(scramble code) x (1 + 2 x M) (timings)] by using the previous cell search result proposed by this invention although redetection is carried out to the timings of M samples before and after. Accordingly, it is possible to carry out the cell search in the same cell at a high speed and to decrease a consumed power.

Referring to Fig. 4, the description will proceed to a main part (a cell search circuit) of the mobile station MS which realizes a cell search method according to a second embodiment of this invention. The illustrated cell search circuit can achieve a high-speed processing and decreasing of the consumed power not only on re-cell search processing in the same sector but also on re-cell search processing in the same cell with an inter-sector movement by taking a timing offset between sectors in the same cell into consideration.

The illustrated cell search circuit is similar in structure and operation to that illustrated in Fig. 1 except that the cell search circuit further comprises a spreading

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timing controlling circuit 18. Accordingly, the same reference symbols are attached to those having similar functions to those illustrated in Fig. 1. The cell search circuit illustrated in Fig. 4 uses a first communication stop time interval threshold value T_{max1} and a second communication stop time interval threshold value T_{max2} which is longer than the first communication stop time interval threshold value T_{max1} .

If the timer value of the timer 17 is less (shorter) than the first communication stop time interval threshold value T_{max1} on starting of re-communication, the delay profile calculating circuit 12 calculates the delay profile only near to the spreading timing stored in the spreading code and spreading timing memory circuit 15.

On the other hand, it will be assumed that the timer value of the timer 17 is not less (shorter) than the first communication stop time interval threshold value T_{max1} and is less (shorter) than the second communication stop time interval threshold value T_{max2} . In this event, the spreading timing controlling circuit 18 generates spreading timings which take account of the spreading timing stored in the spreading code and spreading timing memory circuit 15 and timing offsets between sectors. By carrying out the cell search processing near to the generated spreading timings, it is possible to achieve a high-speed processing and decreasing of the consumed power in the re-cell search processing when the mobile station MS moves between the sectors in the same cell.

In addition, if the timer value of the timer 17 is not less (shorter) than the second communication stop time interval threshold value T_{max2} , the normal cell search processing is carried out by generating the known signal replicas for the N codes in the known signal replica generating circuit 16.

While this invention has thus far been described in conjunction with a few preferred embodiments thereof, it will now be readily possible for those skilled in the art to put this invention into various other manners. For example, only one communication stop time interval threshold value T_{max} may be used in the second embodiment although the first and the second communication stop time interval threshold values T_{max1} and T_{max2} are used in the above-mentioned second embodiment. In this event, when the timer value of the timer 17 is shorter than the communication stop time interval threshold value T_{max} on starting of re-communication, the cell search is carried out in consideration of the timing offset between the sectors by the spreading timing controlling circuit 18. Although this case may expect a similar merit in the above-mentioned second embodiment, an unnecessary processing is carried out in a case of the re-communication in the same sector. However, this case has a merit where control is simplified.

In addition, it is possible to more correctly carry out control by determining the re-communication in the same sector (cell) by using not only the communication stop time interval but also a moving speed of the mobile station MS. In this event, the moving speed may be estimated by using a fading pitch or the like from the received data and a moving distance may be

estimated on the basis of the estimated moving speed and the timer value. By taking the moving speed into consideration, it is possible to more correctly estimate the moving distance in comparison with determination of use of only time. That is, it is possible to more correctly determine whether or not the re-communication in the same sector (cell).

WHAT IS CLAIMED IS:

1. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the step of carrying out a cell search processing by using cell search result information on previous communication.

2. A method as claimed in claim 1, wherein said method further comprises the steps of:

measuring, by a timer, an elapsed time interval between an end of communication and a start of re-communication; and determining, on the basis of said elapsed time interval, whether or not uses the cell search result information on said previous communication should be used.

3. A method as claimed in claim 1, wherein said method further comprises the steps of:

measuring, by a timer, an elapsed time interval between an end of communication and a start of re-communication; estimating a moving speed of a mobile station; estimating a moving distance on the basis of the estimated moving speed and said elapsed time interval; and determining, on the basis of the estimated moving distance, whether or not the cell search result information on said previous communication should be used.

4. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the step of:

storing, on ending communication, a perch channel spreading code in a memory circuit; and

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carrying out, on starting the next communication, a cell search processing by using the perch channel spreading code stored in said memory circuit.

5. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the step of:

starting a timer on ending communication;

determining, by watching a timer value of said timer on starting the next communication, whether or not the timer value is not less than a communication stop time interval threshold value; and

carrying out a cell search processing using a cell searching result on previous communication when said timer value is less than said communication stop time interval threshold value.

6. A method as claimed in claim 5, wherein said method further comprises the step of carrying out a normal cell search processing when said timer value is not less than said communication stop time interval threshold value.

7. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the steps of:

monitoring a communication stop time interval; and

carrying out a cell search processing using a previous cell search result when said communication stop time interval is shorter than a threshold time interval.

8. A method as claimed in claim 7, wherein said method further comprises the step of carrying out a normal cell search

processing when said communication stop time interval is not less shorter said threshold time interval.

9. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the steps of:

monitoring a communication stop time interval;

carrying out a cell search processing using a previous cell search result when said communication stop time interval is shorter than a first threshold time interval; and

carrying out a cell search processing using said previous cell search result in consideration of a timing offset between respective sectors when said communication stop time interval is not shorter than said first threshold time interval and is shorter than a second threshold time interval.

10. A method as claimed in claim 9, wherein said method further comprises the step of carrying out a normal cell search processing when said communication stop time interval is not shorter than said second threshold time interval.

11. A method of searching a cell in a code division multiple access (CDMA) system, said method comprising the steps of:

monitoring a communication stop time interval;

carrying out a cell search processing using a previous cell search result in consideration of a timing offset between respective sectors when said communication stop time interval is not shorter than a threshold time interval.

12. A method as claimed in claim 11, wherein said method further comprises the step of carrying out a normal cell search

processing when said communication stop time interval is not shorter than said threshold time interval.

13. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

delay profile calculating means for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating means producing a delay profile signal indicative of said N delay profiles;

spreading code and spreading timing detecting means, connected to said delay profile calculating means, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

received data processing means, connected to said spreading code and spreading timing detecting means, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

spreading code and spreading timing memory means, connected to said spreading code and spreading timing detecting means, for storing information of the using spreading code and the using spreading timing represented by said spreading code

and spreading timing detected signal therein, said spreading code and spreading timing memory means producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval; and

known signal replica generating means connected to said timer, said spreading code and spreading timing detecting means, said spreading code and spreading timing memory means, and said delay profile calculating means, said known signal replica generating means supplying said known signal replicas for N codes to said delay profile calculating means to make a normal cell search processing carry out when said timer value is not less than a communication stop time interval threshold value on starting of re-communication, said known signal replica generating means making said delay profile calculating means generate a delay profile near to the spreading timing on a previous communication by using only one spreading code stored in said spreading code and spreading timing memory means when said timer value is less than the communication stop time interval threshold value on staring of the re-communication.

14. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

delay profile calculating means for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is

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not less than two, said delay profile calculating means producing a delay profile signal indicative of said N delay profiles;

spreading code and spreading timing detecting means, connected to said delay profile calculating means, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

received data processing means, connected to said spreading code and spreading timing detecting means, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

spreading code and spreading timing memory means, connected to said spreading code and spreading timing detecting means, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory means producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval;

spreading timing controlling means, connected to said spreading code and spreading timing memory means, for generating spreading timings in consideration of the spreading

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timing stored in said spreading code and spreading timing memory means and a timing offset between sectors; and

known signal replica generating means connected to said timer, said spreading code and spreading timing detecting means, said spreading code and spreading timing memory means, and said delay profile calculating means, said known signal replica generating means making said delay profile calculating means generate a delay profile only near to the spreading timing stored in said spreading code and spreading timing memory means when said timer value is less than a first communication stop time interval threshold value on starting of a re-communication, said known signal replica generating means making said delay profile calculating means carry out a cell search processing near to the spreading timings generated by said spreading timing controlling means when said timer value is not less than said first communication stop time interval threshold value and is less than a second communication stop time interval threshold value on starting of the re-communication, said known signal replica generating means supplying said known signal replicas for N codes to said delay profile calculating means to make a normal cell search processing carry out when said timer value is not less than said second communication stop time interval threshold value on starting of the re-communication.

15. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

delay profile calculating means for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature

component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating means producing a delay profile signal indicative of said N delay profiles;

spreading code and spreading timing detecting means, connected to said delay profile calculating means, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

received data processing means, connected to said spreading code and spreading timing detecting means, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

spreading code and spreading timing memory means, connected to said spreading code and spreading timing detecting means, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory means producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval;

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spreading timing controlling means, connected to said spreading code and spreading timing memory means, for generating spreading timings in consideration of the spreading timing stored in said spreading code and spreading timing memory means and a timing offset between sectors; and

known signal replica generating means connected to said timer, said spreading code and spreading timing detecting means, said spreading code and spreading timing memory means, and said delay profile calculating means, said known signal replica generating means making said delay profile calculating means carry out a cell search processing near to the spreading timings generated by said spreading timing controlling means when said timer value is not less than a communication stop time interval threshold value on starting of re-communication, said known signal replica generating means supplying said known signal replicas for N codes to said delay profile calculating means to make a normal cell search processing carry out when said timer value is not less than said communication stop time interval threshold value on starting of the re-communication.

16. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

a delay profile calculating circuit for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating circuit producing a delay profile signal indicative

of said N delay profiles;

a spreading code and spreading timing detecting circuit, connected to said delay profile calculating circuit, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

a received data processing circuit, connected to said spreading code and spreading timing detecting circuit, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

a spreading code and spreading timing memory circuit, connected to said spreading code and spreading timing detecting circuit, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory circuit producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval; and

a known signal replica generating circuit connected to said timer, said spreading code and spreading timing detecting circuit, said spreading code and spreading timing memory circuit, and said delay profile calculating circuit, said known signal replica generating circuit supplying said known signal

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replicas for N codes to said delay profile calculating circuit to make a normal cell search processing carry out when said timer value is not less than a communication stop time interval threshold value on starting of re-communication, said known signal replica generating circuit making said delay profile calculating circuit generate a delay profile near to the spreading timing on a previous communication by using only one spreading code stored in said spreading code and spreading timing memory circuit when said timer value is less than the communication stop time interval threshold value on staring of the re-communication.

17. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

a delay profile calculating circuit for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating circuit producing a delay profile signal indicative of said N delay profiles;

a spreading code and spreading timing detecting circuit, connected to said delay profile calculating circuit, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

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a received data processing circuit, connected to said spreading code and spreading timing detecting circuit, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

a spreading code and spreading timing memory circuit, connected to said spreading code and spreading timing detecting circuit, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory circuit producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval;

a spreading timing controlling circuit, connected to said spreading code and spreading timing memory circuit, for generating spreading timings in consideration of the spreading timing stored in said spreading code and spreading timing memory circuit and a timing offset between sectors; and

a known signal replica generating circuit connected to said timer, said spreading code and spreading timing detecting circuit, said spreading code and spreading timing memory circuit, and said delay profile calculating circuit, said known signal replica generating circuit making said delay profile calculating circuit generate a delay profile only near to the spreading timing stored in said spreading code and spreading timing memory circuit when said timer value is less than a first

communication stop time interval threshold value on starting of a re-communication, said known signal replica generating circuit making said delay profile calculating circuit carry out a cell search processing near to the spreading timings generated by said spreading timing controlling circuit when said timer value is not less than said first communication stop time interval threshold value and is less than a second communication stop time interval threshold value on starting of the re-communication, said known signal replica generating circuit supplying said known signal replicas for N codes to said delay profile calculating circuit to make a normal cell search processing carry out when said timer value is not less than said second communication stop time interval threshold value on starting of the re-communication.

18. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

a delay profile calculating circuit for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating circuit producing a delay profile signal indicative of said N delay profiles;

a spreading code and spreading timing detecting circuit, connected to said delay profile calculating circuit, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak

of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

a received data processing circuit, connected to said spreading code and spreading timing detecting circuit, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

a spreading code and spreading timing memory circuit, connected to said spreading code and spreading timing detecting circuit, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory circuit producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval;

a spreading timing controlling circuit, connected to said spreading code and spreading timing memory circuit, for generating spreading timings in consideration of the spreading timing stored in said spreading code and spreading timing memory circuit and a timing offset between sectors; and

a known signal replica generating circuit connected to said timer, said spreading code and spreading timing detecting circuit, said spreading code and spreading timing memory circuit, and said delay profile calculating circuit, said known signal replica generating circuit making said delay profile

calculating circuit carry out a cell search processing near to the spreading timings generated by said spreading timing controlling circuit when said timer value is not less than a communication stop time interval threshold value on starting of re-communication, said known signal replica generating circuit supplying said known signal replicas for N codes to said delay profile calculating circuit to make a normal cell search processing carry out when said timer value is not less than said communication stop time interval threshold value on starting of the re-communication.

Abstract of the Disclosure:

On ending communication, a timer (17) is started in order to watch a communication stop time interval (S1, S2). On staring the next communication, a timer value of the timer is watched (S5). If the timer value is less than a communication stop time interval threshold value, a cell search processing is carried out by using a cell search result on previous communication (S7). By monitoring a communication stop time interval and by using a previous cell search result in the manner described above, a cell search circuit has an important function which realizes a high-speed cell search in the same sector (the same cell) on continuous communications and decreasing of a consumed power.

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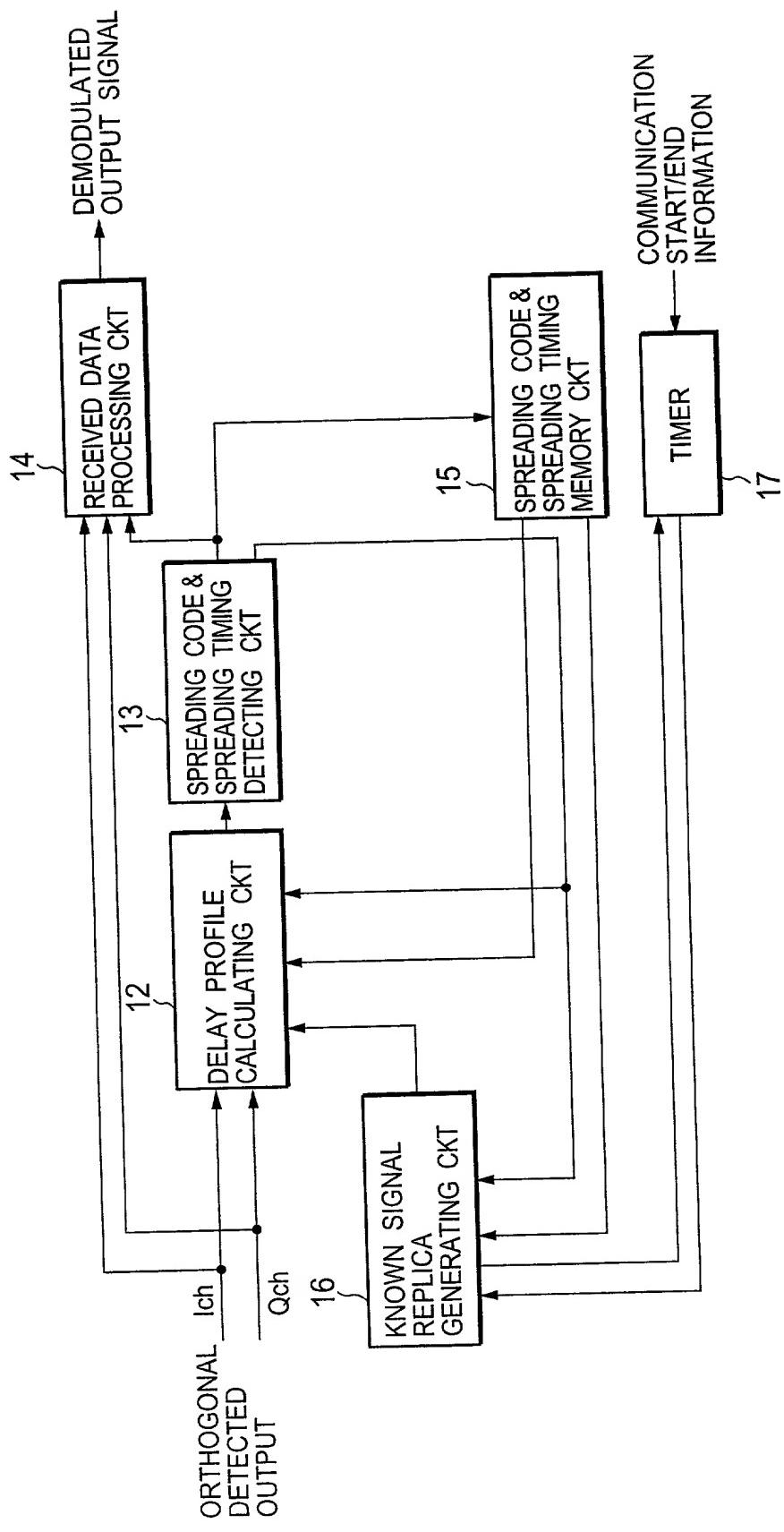


FIG. 1

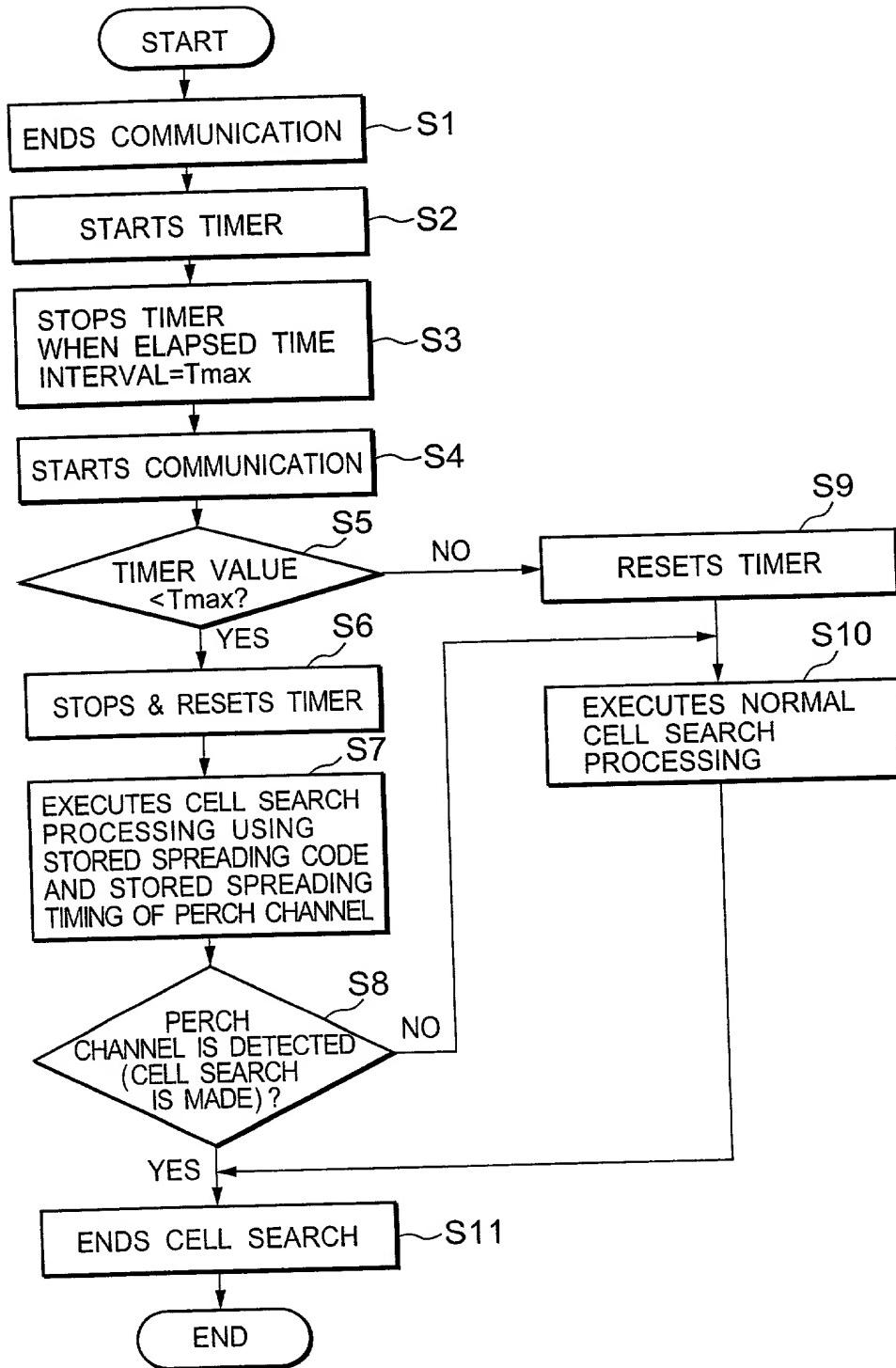


FIG.2

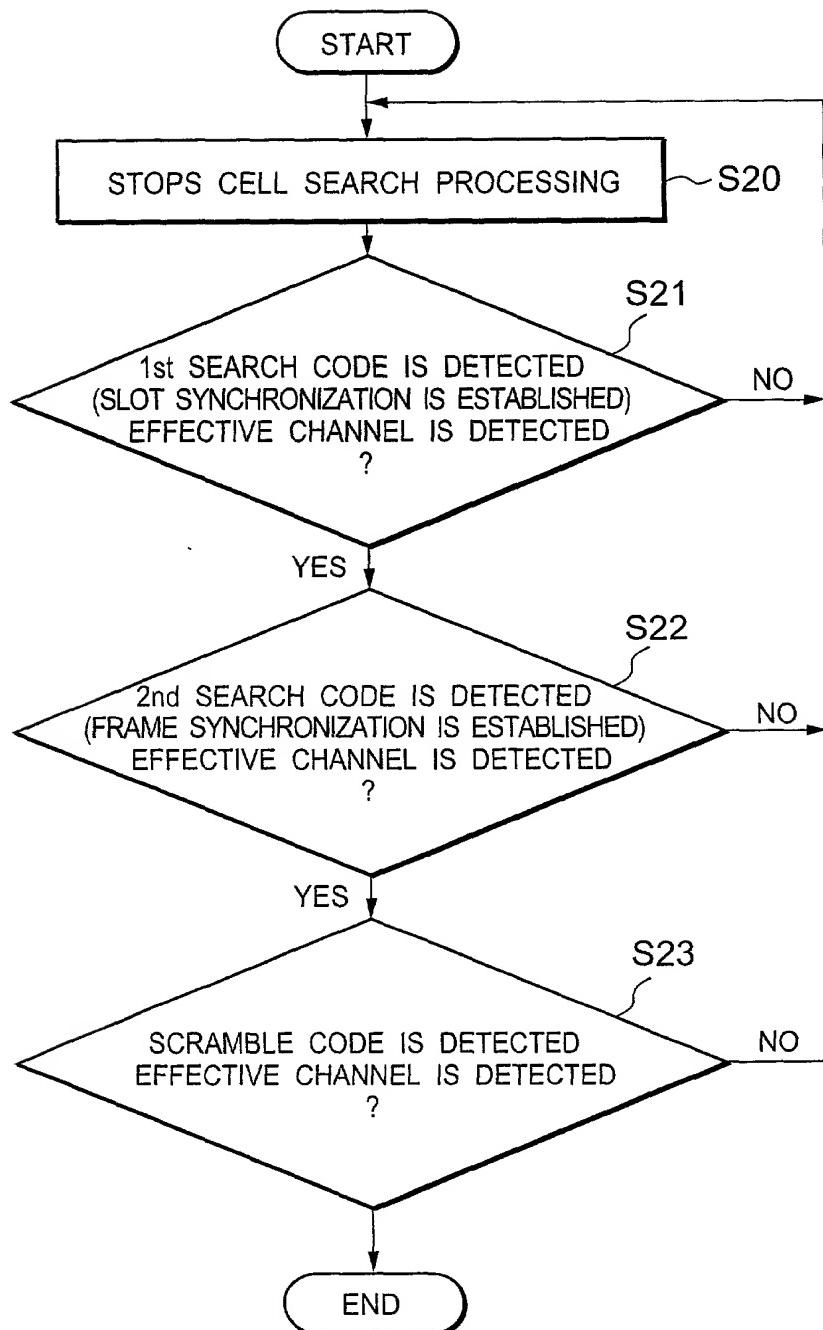


FIG.3 PRIOR ART

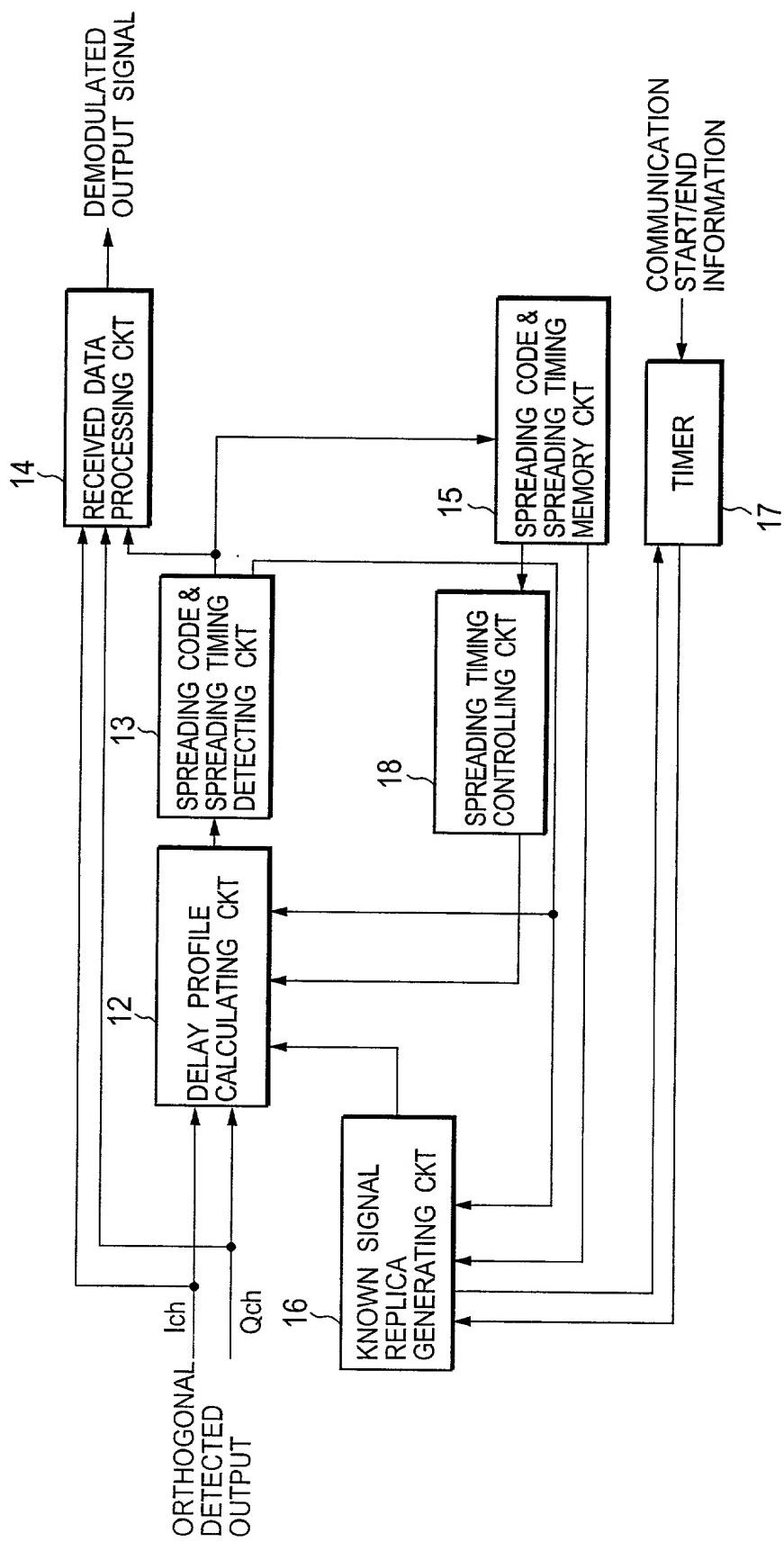


FIG.4

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DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I HEREBY DECLARE:

THAT my residence, post office address, and citizenship are as stated below next to my name,

THAT I believe I am the original, first, and sole inventor (if only one inventor is named below) or an original, first, and joint inventor (if plural inventors are named below or in an attached Declaration) of the subject matter which is claimed and for which a patent is sought on the invention entitled

CELL SEARCH METHOD IN CDMA CAPABLE OF CARRYING OUT

A CELL SEARCH PROCESSING AT A HIGH SPEED

the specification of which (check one)

x

is attached hereto.

was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

THAT I do not know and do not believe that the same invention was ever known or used by others in the United States of America, or was patented or described in any printed publication in any country, before I (we) invented it;

THAT I do not know and do not believe that the same invention was patented or described in any printed publication in any country, or in public use or on sale in the United States of America, for more than one year prior to the filing date of this United States application;

THAT I do not know and do not believe that the same invention was first patented or made the subject of an inventor's certificate that issued in any country foreign to the United States of America before the filing date of this United States application if the foreign application was filed by me (us), or by my (our) legal representatives or assigns, more than twelve months (six months for design patents) prior to the filing date of this United States application;

THAT I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment specifically referred to above;

THAT I believe that the above-identified specification contains a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is

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most nearly connected, to make and use the invention, and sets forth the best mode contemplated by me of carrying out the invention; and

THAT I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, §1.56.

I HEREBY CLAIM foreign priority benefits under Title 35, United States Code §119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or §365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number	Country	Foreign Filing Date	Priority Claimed?	Certified Copy Attached?
11-260461	Japan	September 14, 1999	yes	yes

I HEREBY CLAIM the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below.

U S Provisional Application Number	Filing Date

I HEREBY CLAIM the benefit under Title 35, United States Code, §120 of any United States application(s), or § 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

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U S Parent Application Number	PCT Parent Application Number	Parent Filing Date	Parent Patent Number

I HEREBY APPOINT the following registered attorneys and agents of the law firm of FOLEY & LARDNER to have full power to prosecute this application and any continuations, divisions, reissues, and reexaminations thereof, to receive the patent, and to transact all business in the United States Patent and Trademark Office connected therewith:

STEPHEN A BENT	Reg No	29,768
DAVID A BLUMENTHAL	Reg No	26,257
BETH A BURROUS	Reg No	35,087
ALAN I CANTOR	Reg No	28,163
WILLIAM T ELLIS	Reg No	26,874
JOHN J FELDHAUS	Reg No	28,822
PATRICIA D GRANADOS	Reg No	33,683
JOHN P ISACSON	Reg No	33,715
MICHAEL D KAMINSKI	Reg No	32,904
LYLE K KIMMS	Reg No	34,079
KENNETH E KROSIN	Reg No	25,735
JOHNNY A KUMAR	Reg No	34,649
GLENN LAW	Reg No	34,371
PETER G MACK	Reg No	26,001
BRIAN J MC NAMARA	Reg No	32,789
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RICHARD C PEET	Reg No	35,792
GEORGE E QUILLIN	Reg No	32,792
COLIN G SANDERCOCK	Reg No	31,298
BERNHARD D SAXE	Reg No	28,665
CHARLES F SCHILL	Reg No	27,590
RICHARD L SCHWAAB	Reg No	25,479
ARTHUR SCHWARTZ	Reg No	22,115
HAROLD C WEGNER	Reg No	25,258

and I request that all correspondence be directed to:

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3000 K Street, N.W., Suite 500
Washington, D.C. 20007-5109

Telephone: 202-672-5407
Facsimile: 202-672-5399

I UNDERSTAND AND AGREE THAT the foregoing attorneys and agents appointed by me to prosecute this application do not personally represent me or my legal interests, but instead represent the interests of the legal owner(s) of the invention described in this application.

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I FURTHER DECLARE THAT all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Name of first inventor KOICHI TAMURA

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Inventor's signature Koichi Tamura



Date September 8, 2000

Name of second inventor _____

Residence _____

Citizenship _____

Post Office Address _____

Inventor's signature _____

Date _____

Name of third inventor _____

Residence _____

Citizenship _____

Post Office Address _____

Inventor's signature _____

Date _____